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EXAMINER
HAILE, FEBEN

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NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patent-ch@btlaw.com

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>03 January 2008</u>.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-28</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1-28</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on <u>03 January 2008</u> is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1.   In view of applicant's amendment filed January 03, 2008, the status of the

application is still pending with respect to claims 1-28.

2.   The amendment filed is insufficient to overcome the rejection of claims 1-28

based upon Applicants Admitted Prior Art, (see background of the invention, pages 1-3),

Ridings (US 6,615,310), and Chen (US 2002/0156990) as set forth in this Office action

because: the material added to the claims fail to further clarify a distinction between the

Applicants invention and the cited reference, thus the subject matter is not patentable.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3.   Claims 1, 3-8, 10, 12-17, 19, 21-26, and 28 rejected under 35 U.S.C. 103(a) as

being unpatentable over Applicants Admitted Prior Art, (see background of the

invention, pages 1-3), hereinafter referred to as AAPA, in view of Ridings (US

6,615,310), hereinafter referred to as Riding.

Regarding claim 1, AAPA discloses (i) writing a block of data to an area of a

buffer as a plurality of rows **(page 2 line 30-page 3 line 5; a block of CAS data is**

written to a first buffer in series), each row comprising a predetermined number of timeslots of data **(page 1 line 34-page 2 line 4; in the E1 standard, a timeslot of a CAS block for each trunk is received every 125 μs, a CAS block equals 32 rows of data that corresponds to 32 communication channels of each trunk, thus each row contains a timeslot for a communication channel of each trunk)**; (ii) writing a next block of data to an area of the circular memory buffer located sequentially after the area occupied by the previous block of data as a plurality of rows **(page 2 line 30-page 3 line 5; a block of CAS data is written to a second buffer in series)**, each row comprising a predetermined number of timeslots of data, wherein after writing each row of said next block of data **(page 1 line 34-page 2 line 4; in the E1 standard, a timeslot of a CAS block for each trunk is received every 125 μs, a CAS block equals 32 rows of data that corresponds to 32 communication channels of each trunk, thus each row contains a timeslot for a communication channel of each trunk)**, changes in the data contained in the row are determined by comparing the row with the corresponding row in the previous block of data **(page 3 lines 7-13; changes in the block of data are compared to a previous block of data)**; and (iii) repeating step (ii) a plurality of times **(page 3 lines 24-25; this method is continued in a loop for as long as data is being received and monitored)**.

AAPA discloses the claimed invention except for the buffer being a circular memory. It would have been obvious to one having ordinary skill in the art at the time the invention was made that to use a circular type of memory is a manner of design choice. An advantage of using such a buffer being, to bridge the constant sample data

rate of input and output with a DSP processor, which is commonly programmed to process entire blocks of data at one time.

AAPA fails to explicitly suggest wherein the comparing of a first row is commenced before the last row has been written.

Ridings teaches wherein the comparing of a first row is commenced before the last row has been written **(column 6 lines 34-39; all CAM words are available for comparison while also writing new data into the current CAM word, i.e. fig. 3, while a word is being written into location 303, the word is also compared to previously written words in location 301-302)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the method of CAM write and compare function taught by Ridings into the method of CAS bit change detection disclosed by AAPA. The motivation for such a modification is increasing the likelihood of matching the current CAM location, thus more efficiently compressing data.

Regarding claim 3, AAPA discloses wherein data is written to the circular memory buffer by direct memory access (DMA) **(page 2 lines 30-31; the blocks of data are written to the first and second buffers by a DMA)**.

Regarding claim 4, AAPA discloses wherein, in step (ii), after writing each row of the block of data, an interrupt is generated, and wherein changes in the data contained in the row are determined in response to the interrupt **(page 3 lines 7-13; once a complete block of data has been written to one of the first or second buffers, changes in the block of data is compared to a previous block of data)**.

Regarding claim 5, AAPA discloses wherein a row of data is written to the circular memory buffer every 125 µs **(page 1 line34-page 2 line 1; In the E1 standard, a time slot of CAS data is received every 125 µs, thus its obvious to one of ordinary skill in the art that the data would be written into the buffer at the same rate)**.

Regarding claim 6, AAPA discloses wherein all blocks of data are alternately written to one of two areas of the circular memory **buffer (page 3 lines 1-2; alternate blocks of data are written to each of the first and second buffers so that only one buffer is written at any one time)**.

Regarding claim 7, AAPA discloses the claimed invention except wherein the size of each areas of the circular memory buffer is equal to the size of a block of data. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that a CAS block equals 24 or 32 rows of data, depending on E1 or T1 standards, thus the size of the buffer would at least have to be large enough to write that amount of data.

Regarding claim 8, AAPA discloses wherein the locations of the two areas of the circular memory buffer are consecutive **(page 2 line 30-page 3 line 5; blocks of CAS data are written to first and second buffers alternately in series; thus it would have been obvious to one having ordinary skill in the art that the two buffers are successive)**.

Regarding claim 10, AAPA discloses (i) writing a block of data to an area of a buffer as a plurality of rows **(page 2 line 30-page 3 line 5; a block of CAS data is**

written to a first buffer in series), each row comprising a predetermined number of

timeslots of data **(page 1 line 34-page 2 line 4; in the E1 standard, a timeslot of a**

CAS block for each trunk is received every 125 μs, a CAS block equals 32 rows of

data that corresponds to 32 communication channels of each trunk, thus each

row contains a timeslot for a communication channel of each trunk); (ii) writing a

next block of data to an area of the circular memory buffer located sequentially after the

area occupied by the previous block of data as a plurality of rows **(page 2 line 30-page**

3 line 5; a block of CAS data is written to a second buffer in series), each row

comprising a predetermined number of timeslots of data, wherein after writing each row

of said next block of data **(page 1 line 34-page 2 line 4; in the E1 standard, a**

timeslot of a CAS block for each trunk is received every 125 μs, a CAS block

equals 32 rows of data that corresponds to 32 communication channels of each

trunk, thus each row contains a timeslot for a communication channel of each

trunk), changes in the data contained in the row are determined by comparing the row

with the corresponding row in the previous block of data **(page 3 lines 7-13; changes**

in the block of data are compared to a previous block of data); and (iii) repeating

step (ii) a plurality of times **(page 3 lines 24-25; this method is continued in a loop**

for as long as data is being received and monitored).

AAPA discloses the claimed invention except for the buffer being a circular

memory. It would have been obvious to one having ordinary skill in the art at the time

the invention was made that to use a circular type of memory is a manner of design

choice. An advantage of using such a buffer being, to bridge the constant sample data

rate of input and output with a DSP processor, which is commonly programmed to process entire blocks of data at one time.

AAPA fails to explicitly suggest wherein the comparing of a first row is commenced before the last row has been written.

Ridings teaches wherein the comparing of a first row is commenced before the last row has been written **(column 6 lines 34-39; all CAM words are available for comparison while also writing new data into the current CAM word, i.e. fig. 3, while a word is being written into location 303, the word is also compared to previously written words in location 301-302)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the method of CAM write and compare function taught by Ridings into the method of CAS bit change detection disclosed by AAPA. The motivation for such a modification is increasing the likelihood of matching the current CAM location, thus more efficiently compressing data.

Regarding claim 12, AAPA discloses wherein data is written to the circular memory buffer by direct memory access (DMA) **(page 2 lines 30-31; the blocks of data are written to the first and second buffers by a DMA)**.

Regarding claim 13, AAPA discloses wherein, in step (ii), after writing each row of the block of data, an interrupt is generated, and wherein changes in the data contained in the row are determined in response to the interrupt **(page 3 lines 7-13; once a complete block of data has been written to one of the first or second buffers, changes in the block of data is compared to a previous block of data)**.

Regarding claim 14, AAPA discloses wherein a row of data is written to the circular memory buffer every 125 µs **(page 1 line34-page 2 line 1; In the E1 standard, a time slot of CAS data is received every 125 µs, thus its obvious to one of ordinary skill in the art that the data would be written into the buffer at the same rate)**.

Regarding claim 15, AAPA discloses wherein all blocks of data are alternately written to one of two areas of the circular memory **buffer (page 3 lines 1-2; alternate blocks of data are written to each of the first and second buffers so that only one buffer is written at any one time)**.

Regarding claim 16, AAPA discloses the claimed invention except wherein the size of each areas of the circular memory buffer is equal to the size of a block of data. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that a CAS block equals 24 or 32 rows of data, depending on E1 or T1 standards, thus the size of the buffer would at least have to be large enough to write that amount of data.

Regarding claim 17, AAPA discloses wherein the locations of the two areas of the circular memory buffer are consecutive **(page 2 line 30-page 3 line 5; blocks of CAS data are written to first and second buffers alternately in series; thus it would have been obvious to one having ordinary skill in the art that the two buffers are successive)**.

Regarding claim 19, AAPA discloses (i) write a block of data to an area of a buffer as a plurality of rows **(page 2 line 30-page 3 line 5; a block of CAS data is**

written to a first buffer in series), each row comprising a predetermined number of

timeslots of data **(page 1 line 34-page 2 line 4; in the E1 standard, a timeslot of a**

CAS block for each trunk is received every 125 μs, a CAS block equals 32 rows of

data that corresponds to 32 communication channels of each trunk, thus each

row contains a timeslot for a communication channel of each trunk); (ii) write a

next block of data to an area of the circular memory buffer located sequentially after the

area occupied by the previous block of data as a plurality of rows **(page 2 line 30-page**

3 line 5; a block of CAS data is written to a second buffer in series), each row

comprising a predetermined number of timeslots of data, wherein after writing each row

of said next block of data **(page 1 line 34-page 2 line 4; in the E1 standard, a**

timeslot of a CAS block for each trunk is received every 125 μs, a CAS block

equals 32 rows of data that corresponds to 32 communication channels of each

trunk, thus each row contains a timeslot for a communication channel of each

trunk), changes in the data contained in the row are determined by comparing the row

with the corresponding row in the previous block of data **(page 3 lines 7-13; changes**

in the block of data are compared to a previous block of data); and (iii) repeat step

(ii) a plurality of times **(page 3 lines 24-25; this method is continued in a loop for as**

long as data is being received and monitored).

AAPA discloses the claimed invention except for the buffer being a circular

memory. It would have been obvious to one having ordinary skill in the art at the time

the invention was made that to use a circular type of memory is a manner of design

choice. An advantage of using such a buffer being, to bridge the constant sample data

rate of input and output with a DSP processor, which is commonly programmed to process entire blocks of data at one time.

AAPA fails to explicitly suggest wherein the comparing of a first row is commenced before the last row has been written.

Ridings teaches wherein the comparing of a first row is commenced before the last row has been written **(column 6 lines 34-39; all CAM words are available for comparison while also writing new data into the current CAM word, i.e. fig. 3, while a word is being written into location 303, the word is also compared to previously written words in location 301-302)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the method of CAM write and compare function taught by Ridings into the method of CAS bit change detection disclosed by AAPA. The motivation for such a modification is increasing the likelihood of matching the current CAM location, thus more efficiently compressing data.

Regarding claim 21, AAPA discloses data is written to the circular memory buffer by direct memory access (DMA) **(page 2 lines 30-31; the blocks of data are written to the first and second buffers by a DMA)**.

Regarding claim 22, AAPA discloses in step (ii), after writing each row of the block of data, an interrupt is generated, and wherein changes in the data contained in the row are determined in response to the interrupt **(page 3 lines 7-13; once a complete block of data has been written to one of the first or second buffers, changes in the block of data is compared to a previous block of data)**.

Regarding claim 23, AAPA discloses a row of data is written to the circular memory buffer every 125 µs **(page 1 line34-page 2 line 1; In the E1 standard, a time slot of CAS data is received every 125 µs, thus its obvious to one of ordinary skill in the art that the data would be written into the buffer at the same rate)**.

Regarding claim 24, AAPA discloses all blocks of data are alternately written to one of two areas of the circular memory **buffer (page 3 lines 1-2; alternate blocks of data are written to each of the first and second buffers so that only one buffer is written at any one time)**.

Regarding claim 25, AAPA discloses the claimed invention except wherein the size of each areas of the circular memory buffer is equal to the size of a block of data. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that a CAS block equals 24 or 32 rows of data, depending on E1 or T1 standards, thus the size of the buffer would at least have to be large enough to write that amount of data.

Regarding claim 26, AAPA discloses the locations of the two areas of the circular memory buffer are consecutive **(page 2 line 30-page 3 line 5; blocks of CAS data are written to first and second buffers alternately in series; thus it would have been obvious to one having ordinary skill in the art that the two buffers are successive)**.

Regarding claim 28, AAPA discloses (i) write a block of data to an area of a buffer as a plurality of rows **(page 2 line 30-page 3 line 5; a block of CAS data is written to a first buffer in series)**, each row comprising a predetermined number of

timeslots of data **(page 1 line 34-page 2 line 4; in the E1 standard, a timeslot of a CAS block for each trunk is received every 125 μs, a CAS block equals 32 rows of data that corresponds to 32 communication channels of each trunk, thus each row contains a timeslot for a communication channel of each trunk)**; (ii) write a next block of data to an area of the circular memory buffer located sequentially after the area occupied by the previous block of data as a plurality of rows **(page 2 line 30-page 3 line 5; a block of CAS data is written to a second buffer in series)**, each row comprising a predetermined number of timeslots of data, wherein after writing each row of said next block of data **(page 1 line 34-page 2 line 4; in the E1 standard, a timeslot of a CAS block for each trunk is received every 125 μs, a CAS block equals 32 rows of data that corresponds to 32 communication channels of each trunk, thus each row contains a timeslot for a communication channel of each trunk)**, changes in the data contained in the row are determined by comparing the row with the corresponding row in the previous block of data **(page 3 lines 7-13; changes in the block of data are compared to a previous block of data)**; and (iii) repeat step (ii) a plurality of times **(page 3 lines 24-25; this method is continued in a loop for as long as data is being received and monitored)**.

AAPA discloses the claimed invention except for the buffer being a circular memory. It would have been obvious to one having ordinary skill in the art at the time the invention was made that to use a circular type of memory is a manner of design choice. An advantage of using such a buffer being, to bridge the constant sample data

rate of input and output with a DSP processor, which is commonly programmed to process entire blocks of data at one time.

AAPA fails to explicitly suggest wherein the comparing of a first row is commenced before the last row has been written.

Ridings teaches wherein the comparing of a first row is commenced before the last row has been written **(column 6 lines 34-39; all CAM words are available for comparison while also writing new data into the current CAM word, i.e. fig. 3, while a word is being written into location 303, the word is also compared to previously written words in location 301-302).**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the method of CAM write and compare function taught by Ridings into the method of CAS bit change detection disclosed by AAPA. The motivation for such a modification is increasing the likelihood of matching the current CAM location, thus more efficiently compressing data.

4.   Claims 2, 9, 11, 18, 20, and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art, (see background of the invention, pages 1-3), hereinafter referred to as AAPA, in view of Ridings (US 6,615,310), hereinafter referred to as Riding, in view of Chen (US 2002/0156990), hereinafter referred to as Chen

Regarding claim 2, AAPA discloses and comparing the CAS data bits in each timeslot of the row with the CAS data bits in each timeslot of the corresponding row of

the previous block **(page 1 line 34-page 2 line 4; a row, i.e. block of data, including a timeslot of CAS data; page 1 lines 17-20; monitor for changes in bits of CAS data every 4ms; page 3 lines 7-13; changes in the block of data are compared to a previous block of data).**

Riding discloses reading the corresponding row in the previous block **(column 7 lines 1-5; data to be compared, i.e. previous block, is launched, i.e. read)**.

However, AAPA, Ridings, and/or their combination fail to explicitly suggest locating the corresponding row in the previous block by applying a fixed memory offset from the location of the row.

Chen teaches locating the corresponding row in the previous block by applying a fixed memory offset from the location of the row **(figure 3 and page 2 paragraph 0022; deducting all addresses of a circular buffer 304 from a base address N is equivalent to an offset of the circular buffer 304 to the top of a memory 302 into the "virtual" circular buffer 306)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the method for determining a modulus address taught by Chen into the method of CAS bit change detection disclosed by AAPA as modified by the method of CAM write and compare function taught by suggested by Ridings. The motivation for such a modification is a simpler circuit to implement the modulus addressing.

Regarding claim 7, Chen discloses wherein the size of the fixed memory offset is equal to the size of a block of data **(page 3 paragraphs 0031-0047; a separator**

circuit performs an AND Boolean operation applied to S and A via an AND gate to obtain the offset value, where S is generated by the length of the circular buffer).

Regarding claim 11, AAPA discloses and comparing the CAS data bits in each timeslot of the row with the CAS data bits in each timeslot of the corresponding row of the previous block **(page 1 line 34-page 2 line 4; a row, i.e. block of data, including a timeslot of CAS data; page 1 lines 17-20; monitor for changes in bits of CAS data every 4ms; page 3 lines 7-13; changes in the block of data are compared to a previous block of data)**.

Riding discloses reading the corresponding row in the previous block **(column 7 lines 1-5; data to be compared, i.e. previous block, is launched, i.e. read)**.

However, AAPA, Ridings, and/or their combination fail to explicitly suggest locating the corresponding row in the previous block by applying a fixed memory offset from the location of the row.

Chen teaches locating the corresponding row in the previous block by applying a fixed memory offset from the location of the row **(figure 3 and page 2 paragraph 0022; deducting all addresses of a circular buffer 304 from a base address N is equivalent to an offset of the circular buffer 304 to the top of a memory 302 into the "virtual" circular buffer 306)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the method for determining a modulus address taught by Chen into the method of CAS bit change detection disclosed by AAPA as

modified by the method of CAM write and compare function taught by suggested by Ridings. The motivation for such a modification is a simpler circuit to implement the modulus addressing.

Regarding claim 18, Chen discloses wherein the size of the fixed memory offset is equal to the size of a block of data **(page 3 paragraphs 0031-0047; a separator circuit performs an AND Boolean operation applied to S and A via an AND gate to obtain the offset value, where S is generated by the length of the circular buffer)**.

Regarding claim 20, AAPA discloses and comparing the CAS data bits in each timeslot of the row with the CAS data bits in each timeslot of the corresponding row of the previous block **(page 1 line 34-page 2 line 4; a row, i.e. block of data, including a timeslot of CAS data; page 1 lines 17-20; monitor for changes in bits of CAS data every 4ms; page 3 lines 7-13; changes in the block of data are compared to a previous block of data)**.

Riding discloses reading the corresponding row in the previous block **(column 7 lines 1-5; data to be compared, i.e. previous block, is launched, i.e. read)**.

However, AAPA, Ridings, and/or their combination fail to explicitly suggest locating the corresponding row in the previous block by applying a fixed memory offset from the location of the row.

Chen teaches locating the corresponding row in the previous block by applying a fixed memory offset from the location of the row **(figure 3 and page 2 paragraph 0022; deducting all addresses of a circular buffer 304 from a base address N is**

equivalent to an offset of the circular buffer 304 to the top of a memory 302 into the "virtual" circular buffer 306).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the method for determining a modulus address taught by Chen into the method of CAS bit change detection disclosed by AAPA as modified by the method of CAM write and compare function taught by suggested by Ridings. The motivation for such a modification is a simpler circuit to implement the modulus addressing.

Regarding claim 27, Chen discloses wherein the size of the fixed memory offset is equal to the size of a block of data **(page 3 paragraphs 0031-0047; a separator circuit performs an AND Boolean operation applied to S and A via an AND gate to obtain the offset value, where S is generated by the length of the circular buffer).**

Response to Arguments

5.   Applicant's arguments with respect to amending claims 1, 10, 19, and 28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6.   Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

7.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Feben M. Haile whose telephone number is (571) 272-

3072. The examiner can normally be reached on 10:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Aung S. Moe can be reached on (571) 272-7314. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Feben M Haile/   /Aung S. Moe/
Examiner, Art Unit 2616   Supervisory Patent Examiner, Art
                                             Unit 2616